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PATENT APPLICATION:

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Title: FIELD EFFECT TRANSISTOR WITH GATE LAYER AND
METHOD OF MAKING SAME

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BACKGROUND

5 Field of the Invention

10 The present invention relates to field effect transistors (FETs). More particularly, this invention pertains to a field effect transistor having an elongated conductive channel that is inclined with respect to the upper surface of an etched substrate.

Description of the Prior Art

15 Many proposals have been made for making field effect transistors in silicon nanowires. Elongated nanowires of silicon are characterized by diameters on the order of 5 to 30 nanometers, substantially smaller than conventional integrated circuits that include devices having corresponding dimensions on the order of 100 nanometers or more.

20 Efficient modulation of the conductance of the channel region of a nanowire FET requires that the channel region of the nanowire be only moderately doped while the regions external to the active channel (source and drain) should be heavily doped to reduce series resistance. (Generally, a "heavily doped"

25 region is understood by those skilled in the art to be characterized by a sufficient amount of doping to produce a resistivity value of .01 ohm-cm or less (conductivity of 100 (ohm-cm)⁻¹ or more.)

30 Unfortunately, it has been found to be relatively difficult to control absolute dimensions and

5 tolerances at the level of 100 nm or less by conventional lithography processes. In many proposed devices, for example, the distances between the heavily doped regions of the nanowire (if heavily doped regions are employed) and the channel are not well controlled. This leads to high and variable series resistance and/or to regions of abnormally high electric field.

SUMMARY OF THE INVENTION

10 The preceding and other shortcomings of the prior art are addressed by the present invention that provides, in a first aspect, a field effect transistor. Such transistor includes a substrate having a substantially-planar upper substrate surface. An elongated channel of semiconductor material is inclined
15 with respect to the upper substrate surface. The channel includes a top and a bottom with the bottom of the channel contacting the upper substrate surface.

20 The substrate is substantially conductive in the region contacting the bottom of the elongated channel. The channel includes a heavily doped region adjacent the top thereof. A gate comprises a planar layer of conductive material arranged substantially parallel to the upper substrate surface.

25 In a second aspect, the invention provides a method for forming a field effect transistor. Such method is begun by providing a conductive substrate. The substrate is then etched to form an upstanding pillar adjacent a substantially-planar upper surface of the etched substrate.

30 A stack is then formed adjacent the pillar.

5 The stack is of substantially-planar layers of material that include a first insulator layer adjacent the upper surface of the etched substrate, a gate layer of conductive material overlying the first insulator layer and a second insulator layer overlying the gate layer.

10 The pillar is then etched to the level of the substantially-planar upper surface of the etched substrate to form an upstanding pore within the stack. A gate insulator layer is then formed at the interior of the upstanding pore.

15 An upstanding channel of semiconductor material is then formed interior of the gate insulator layer having a top region and a bottom region. Finally, the top region of the upstanding channel is heavily doped.

20 In a third aspect, the invention provides a method for forming a field effect transistor that is begun by providing a substrate of semiconductor material. Such substrate is then etched to form an upstanding pillar adjacent a substantially-planar upper surface of the etched substrate.

25 A conductively-doped region is then formed within the etched substrate substantially and immediately beneath the pillar. A stack is then formed adjacent the pillar of substantially-planar layers of material comprising a first insulator layer adjacent the upper surface of the etched substrate, a gate layer of conductive material overlying the first insulator layer and a second insulator layer overlying the gate layer.

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5 The pillar is then etched to the level of the substantially-planar upper surface of the etched substrate to form an upstanding pore within the stack. A gate insulator layer is then formed interior to the upstanding pore. An upstanding channel of semiconductor material having a top region and a bottom region is then formed interior of the gate insulator layer. Finally, the top region is then heavily doped.

10 In a fourth aspect, the invention provides a method for forming a field effect transistor. The method is begun by providing a substrate having an upper surface. A stack of substantially-planar layers of material is then formed on the substrate. Such stack comprises a first insulator layer adjacent the upper surface of the substrate, a gate layer of conductive material overlying the first insulator layer and a second insulator layer overlying the gate layer.

15 An overlayer is then formed on top of the second insulator layer. The overlayer is then masked with a nanoparticle, then directionally etched to form an upstanding nanopillar on top of the second insulator layer.

20 A second overlayer is then deposited on top of the second insulator layer and the upstanding nanopillar. The second overlayer is then removed to the top of the upstanding nanopillar and the nanopillar is then removed to leave an upper nanopore within the second overlayer defining an etch mask.

25 A lower nanopore is directionally etched through the stack of materials to the upper surface of

the substrate. The second overlayer is then removed and a gate insulator layer is then formed at the interior of the upstanding lower nanopore. An upstanding channel of semiconductor material is then formed interior of the gate insulator layer having a top region and a bottom region. Finally, the top region of the upstanding channel is heavily doped.

The preceding and other features and advantages of the present invention will become apparent from the detailed description that follows. Such description is accompanied by a set of drawing figures. Numerals of the drawing figures, corresponding to those of the written text, point to the features of the invention with like numerals referring to line features throughout both the written text and the drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) through 1(n) are cross-sectional views illustrating resultant structures produced during a process for forming a field effect transistor in accordance with an embodiment of the invention, it being understood that the views illustrated in Figures 1(j) through 1(n) are somewhat enlarged with respect to those of Figures 1(a) through 1(i) for clarity of illustration;

Figures 2(a) through 2(c) are cross-sectional views illustrating the resultant structures produced during a portion of a process for forming a field effect transistor in accordance with an alternative embodiment of the invention; and

5 Figures 3(a) through 3(h) are cross-sectional views of the resultant structures produced during a sequence of process steps for forming a nanopore for use in fabricating a field effect transistor in accordance with an alternative embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

10 The present invention provides a field effect transistor in silicon nanowires in which the distance between the heavily doped regions and the moderately-doped active channel region of the device is well-controlled to thereby overcome problems associated with devices formed by conventional photolithography. This is obtained by a device configuration in which the distance between the highly-doped source and drain regions and a gate electrode is carefully controlled by controlling the thicknesses of deposited layers of material rather than through reliance upon the processes of photolithography to define such regions.

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25 Figures 1(a) through 1(n) are a series of cross-sectional views that illustrate resultant structures formed during a process for making a FET in accordance with an embodiment of the invention. The process is begun by providing a substrate 10. The substrate 10 may be of either a (globally or locally) highly-doped single crystal semiconductor or a single crystal conductor, such as a metal that is capable of supporting epitaxial growth of a channel of semiconductor material. Single crystal silicon is an example of a suitable material.

30

A nanoparticle 12 is applied to the upper

5 surface 14 of the substrate 10 to serve as an etch mask in subsequent processing steps. The nanoparticle 10 can be the result of a dispersion on the surface 14 from the liquid phase or formed by depositing a material of one lattice constant onto a substrate of a different lattice constant and using the forces from the lattice mismatch to form a nanoparticle island.

10 Nanoparticles of well controlled dimensions are readily available. One source, Ted Pella, Inc. of Redding, California, provides gold nanoparticles in a sol with gold particles available in specific sizes ranging from about 2 nm to 250 nm. Such nanoparticles are usually composed of an inorganic crystalline core, typically a metal, that is coated with an organic species to keep the nanoparticles from agglomerating. 15 While the formation of a single FET is illustrated, requiring the formation of a single nanopore and, hence, employing only a single nanoparticle as etch mask, it will be appreciated by those skilled in the art that the following discussion is equally applicable 20 to the formation of a plurality of transistors on a single substrate requiring the distribution of a corresponding plurality of nanoparticles. In such case, the nanoparticles are distributed to a coverage of less than a single layer so that they are separated from one another by a space with no multiple layers of 25 nanoparticles.

30 The nanoparticle 12 acts as an etch mask for the formation of an underlying nanopillar (discussed below) and such nanopillar is eventually etched away to form a nanopore (also discussed below) for accepting various transistor structures. The size of the

nanoparticle 12 (generally in a range of 5 nm to 100 nm) is critical to successful fabrication of the device. By employing a nanoparticle as etch mask, it will be seen to be possible to form a device having a nanowire-sized channel without incurring the substantial expense associated with photolithography.

Returning to the illustrated process for forming a transistor, the structure of Figure 1(b) results from the directional etching of the substrate 10 with the nanoparticle 12 serving as an etch mask. The etch process may comprise reactive ion etching (RIE) to a controlled depth. The etch chemistry and nanoparticle 12 are selected so that the substrate 10 material is etched much more rapidly than the nanoparticle 12. Such etch process results in the creation of an upstanding pillar 16 of the material of the substrate 10 beneath the nanoparticle 12. (Alternatively, a plurality of pillars would result from the distribution of a plurality of nanoparticles onto a surface 14.) While, for most applications, an elongated nanopillar 16 is envisioned whose axis of symmetry is perpendicular to a substantially-planar upper substrate surface 17, other angular orientations are possible and may be accomplished by tilting the substrate 10 prior to directional RIE etching.

As mentioned above, the substrate 10 may comprise a single crystal semiconductor material. The bulk semiconductor may be either moderately or heavily doped. The choice of a conductor or globally heavily doped semiconductor, as opposed to a moderately doped semiconductor will depend upon a number of factors pertaining, in particular, to whether the substrate 10

is to form a common contact (source or drain) region for a plurality of channels of FETs that are to act in parallel (in concert). In such case, the substrate 10 should be either a conductor or a heavily-doped semiconductor material, thereby forming a common source or drain contact, (Note: whether a contact of a FET serves as source or drain depends upon the (external) biasing of the device and is therefore not relevant to the structure or fabrication of a device in accordance with an embodiment of the invention as discussed below.)

In the event that a plurality of FETs, formed on a common substrate 10, are to operate independently of one another, the bulk material of the substrate 10 is not heavily doped. Rather, discrete regions of heavy doping are provided beneath inclined FET channels to form independently-acting transistors on a single substrate 10.

Figure 1(c) illustrates the structure resulting from the formation of a heavily-doped source or drain region 19 within the substrate 10 at the foot of the nanopillar 16 in a device being fabricated to operate independently of at least one other FET being formed in parallel on the common substrate 10. The heavily-doped region 19 is formed through conventional photolithography steps including, for example, masking and ion implantation followed by an anneal step to activate the dopant, causing doped regions to the sides of the upstanding nanopillar 16 (masked by the presence of the nanopillar 16 during ion implantation) to migrate and thereby form the continuous highly-doped region 19 that extends under the nanopillar 16. It may

be noted that the highly-doped region 19 unavoidably extends somewhat into the bottom portion of the nanopillar 16 and is not bounded by the upper surface 17 of the etched substrate 10. This creates no particular problem in a device formed in accordance with an embodiment of the invention as the nanopillar 16 is later removed during processing. This leaves a highly-doped region 19 having a well-defined upper boundary that coincides with the upper surface 17 of the substrate 10. This is to be contrasted with devices in accordance with the prior art, such as a pillar transistor having a substrate and upstanding pillar, formed therewith, that serves as the channel of the device. Such a structure always requires the formation of a highly-doped region that includes an upper portion extending into the pillar whose extent cannot be well controlled. Unlike the case of the present invention, the portion that extends into the upstanding pillar of such a device is not removed during subsequent processing. Consequently, certain problems of the prior art that result from unreliable spacing of source, drain and gate are encountered in such prior art devices.

As the presence or absence of the highly-doped region 19 is not relevant to the following steps, the discussion of the process for fabricating a FET in nanowires will proceed as if the region 19 did not exist and is not illustrated in the subsequent process steps. For this reason, subsequent steps may be assumed to be illustrating a FET formed on a globally conductive or highly-doped substrate 10 in accordance with an embodiment of the invention, taking into consideration that the subsequent processing steps

proceed identically from either of the structures illustrated in Figures 1(b) (no locally defined highly-doped region) and 1(c).

Proceeding to the subsequent processing steps, the structure of Figure 1(d) includes a first insulator layer 18, such as silicon oxide or silicon nitride, that has been deposited to a controlled depth by vapor deposition. This comprises the first step in forming a stack of materials that acts to position a gate layer with great accuracy and to thereby locate the active channel of the device with precision overcoming the effect of inaccuracies in defining the source and drain of the device at opposed regions of the elongated planar (or surface) channel of the FET in prior art devices.

A gate layer 20, forming the second element of the above-mentioned stack, is then deposited over the first insulator layer 18 as shown in Figure 1(e). The layer 20 may comprise either a conductor or a heavily-doped semiconductor material of sufficient thickness to keep the resistance of the transistor control circuitry low. A thickness on the order or range of 10 to 200 nm is appropriate for this purpose.

The gate layer 20 is preferably formed by either a physical or chemical (e.g. using silane, SiH_4 , as source gas) vapor deposition process. Polycrystalline silicon or a high temperature compatible metal, such as tungsten, is an appropriate material for forming the gate layer 20.

After the gate layer 20 has been formed, the

nanoparticle 12, which has acted as an etch mask in prior steps, is shown in the figure to be removed by chemical selective etching and a second insulator layer 22 is deposited to complete the stack 24.

5 (Alternatively, the nanoparticle 12 might be removed during a preceding or subsequent process step. Optimal sequencing of the step of nanoparticle removal will depend upon a number of factors known to those skilled in the art.) Such stack 24 arrangement is illustrated in Figure 1(g). A suitable second insulator layer 22
10 may comprise silicon dioxide or silicon nitride that is preferably vapor deposited.

To expose the top of the nanopillar 16, the upper portion of the second insulating layer 22 is
15 reduced in thickness by, for example, chemical-mechanical polishing (CMP), a technique commonly employed in integrated circuit fabrication. At the end of this process, the upper surface 26 of the second insulating layer 22 is flat and composed of both the
20 exposed top of the nanopillar 16 and the surrounding material of the second insulating layer 22. Figure 1(h) shows the resulting structure after polishing.

A nanopore 28 is formed in the place of the nanopillar 16 as shown in Figure 1(i). The nanopillar
25 16 is removed, preferably by gas-phase etching, leaving the nanopore 28 although other processes might be less-advantageously utilized. Gas phase etching is employed in recognition of the extremely small size of the nanopore 28. While a selective gas phase chemical or
30 plasma etch can remove the nanopillar 16 material without significantly attacking the surrounding materials, one may desire to proceed with the process

in stages, possibly employing a different etching gas as the material of the nanopillar 16 is sequentially removed from adjacent regions of differing physical properties of the stack 24.

5 The preceding steps closely parallel the process disclosed in pending United States patent application Serial No. 10/018,774 of Theodore I. Kamins et al. titled "Method of Forming One or More Nanopores For Aligning Molecules for Molecular Electronics". It
10 differs from the process taught by that application insofar as a stack 24, comprising the first insulator layer 18, the gate layer 20 and the second insulator layer 22, is formed prior to etching the nanopillar 16 to form the nanopore 28. The addition of the
15 conductive gate layer 20 to form the stack 24 will be seen to result in a device in which the location of the active channel of the transistor is clearly defined in relation to source and drain regions. Additionally, by providing a gate layer, electrical contact to the
20 resultant device may be made remote from the channel. As such, problems of high and variable series resistance and regions with abnormally high electric field that result from poor control of the distance between heavily doped regions and the relatively-
25 lightly doped channel are overcome in a device in accordance with an embodiment of the present invention.

 Figure 1(j) illustrates the structure resulting from formation of a conductor layer 30 that
30 lines the interior of the nanopore 28 and forms the gate electrode of the resulting device. The conductor layer 30 contacts the conductive gate layer 20 to define an active channel region that is essentially co-

extensive with the length of a silicon channel
(discussed below) to be formed within the nanopore 28.

5 The conductor layer 30 is preferably metallic
comprising, for example, tungsten or titanium silicide,
although highly-doped polysilicon might also be
employed, and is formed by deposition (a thermally-
activated vapor deposition process is preferred). The
thickness of the conductor layer 30 is related to the
width of the nanopore 28 to assure that adequate space
10 remains for a FET channel. For example, assuming a
nanopore 28 width of 25 nm, the thickness of the
conductive layer 30 would be approximately 5 nm. The
thickness of the conductive layer 30 is a function of
the conductivity of the material of the conductive
15 layer 30. In the case of a very thin conductive layer
30 of high conductivity material, it is preferably
formed by vapor deposition.

Material of the conductive layer 30 is
prevented from depositing on the bottom of the nanopore
20 28 or subsequently removed by, for example, highly
anisotropic etching. This will be seen to prevent the
shorting of the gate of the resultant device.

25 A gate insulator layer 32 is next formed, as
illustrated in Figure 1(k), atop the conductive layer
30. The gate insulator layer 32 may comprise, for
example, SiO_2 of 1.5 nm or greater thickness although
other dielectrics may be employed. Assuming that SiO_2
forms the gate insulator layer 32, a vapor deposition
process is appropriate, preferably chemical rather than
30 physical. As in the case of the conductive layer 30,
the gate insulator layer 32 is prevented from forming

on the bottom of the nanopore 28 or removed by highly anisotropic etching.

5 A channel 34 is then formed within the nanopore 28 as shown in Figure 1(l). The channel 34 may be fabricated of either single crystal or polycrystalline silicon although the size (width) of the void remaining within the nanopore 28 may favor the formation of material without grain boundaries. A chemical vapor deposition process is preferred for forming the channel 34 preferably of single crystal silicon or (if possible) polycrystalline silicon.

15 Despite the above-mentioned caution, one may generally expect the channel 34 to be formed of the same material as the underlying single crystal substrate 10. (Other possibilities for the channel 34 include one of a single crystal semiconductor material differing from the single crystal semiconductor material of the substrate 10 or one of semiconductor material formed on a conductive substrate 10.)

20 Molecular beam epitaxy may alternately be employed to form the channel 34 generally resulting in the same crystalline structure for the channel 34 as that of the substrate 10.

25 The completed FET 36 is illustrated in Figure 1(m). A source or drain region 38 is formed at the top of the channel 34 by heavily doping that region with an appropriate dopant such as boron (p-type), phosphorus (n-type) or arsenic (n-type). Well-known processes, such as ion implantation or gas phase doping processes may be employed. It is generally recognized that the

30 latter type of process generally yields a higher

concentration of dopant.

5 A FET 39 in accordance with the invention is illustrated in Figure 1(n). The device of Figure 1(n) represents the product of the process that comprises steps 1(d) through 1(m) with the highly doped region 19 included. As can be seen, the FET 39 is identical to the FET 36 of Figure 1(m) with the exception of the presence of the highly doped region 19 within a moderately doped semiconductor substrate 10. The
10 differing configuration enables the FET 39 to operate independently of any other FETs that may have also been formed on a common substrate.

15 Figures 2(a) through 2(c) are a series of cross-sectional views for illustrating a portion of a process for forming a field effect transistor in accordance with an alternative embodiment of the invention. The illustrated steps proceed from those illustrated in, and discussed with reference to, Figures 1(a) through 1(i) above.

20 In Figure 2(a), a gate insulator layer 40 is applied to the interior wall of the nanopore 28. In contrast to the prior process, a conductive layer was not previously deposited onto the inner wall of the nanopore 28 as illustrated in Figure 1(j). The absence
25 of a conductive layer results in the gate layer 20 defining the gate electrode of the resultant FET rather than acting solely as a contact to the gate electrode. In the event that the gate layer 20 is of heavily doped polysilicon, the gate insulator layer 40 may be
30 thermally grown. Otherwise, the gate insulator layer 40 is formed by a vapor deposition process.

5 In Figure 2(b), either single crystal silicon or polysilicon is deposited within the nanopore 26 to form a channel 42. The processes and considerations discussed with reference to the process step previously illustrated in conjunction with Figure 1(1) are applicable to the formation of the channel 42 of the alternative embodiment of a transistor in accordance with the invention.

10 The transistor 44 is completed as illustrated in Figure 2(c) by the creation of a heavily-doped region 46 that serves as a source or drain of the transistor. The resultant transistor 44 in accordance with the alternative embodiment of the invention differs from the transistor 36 of the prior embodiment
15 by the absence of a conductive layer 30 and, as mentioned earlier, results in a device in which the gate layer 20 itself serves as the gate electrode. Such a transistor structure possesses certain advantages over the device of the prior embodiment
20 including simpler processing, shorter gate and channel lengths and reduced overlap (source-to-gate, drain-to-gate) capacitance.

25 Alternative process steps for use in forming a transistor in accordance with an embodiment of the invention are illustrated in Figures 3(a) through 3(h). Such alternative steps address the possible difficulty of achieving a uniform multilayer stack 24 adjacent the nanopillar 16.

30 In Figure 3(a), a first insulator layer 18', a gate layer 20' and a second insulator 22' forming a multilayer stack 24' atop a substrate 10' are applied

as described above. Thereafter, as illustrated in Figure 3(b), an overlayer 48 is applied, preferably by vapor deposition over the multilayer stack 24'. The overlayer 48 may comprise insulator, semiconductor or conductor material, preferably of amorphous character. Polycrystalline material is disfavored for the presence of grain boundaries that may introduce complications during subsequent etching of the overlayer 48.

A nanoparticle 12' is applied to the top surface 14' of the overlayer 48 as described with reference to Figure 1(a) above. The overlayer 48 is then directionally etched to form a nanopillar 16' as shown in Figure 3(c). A second overlayer 50 is then deposited as shown in Figure 3(d), covering the top of the nanopillar 16'. In Figure 3(e), the top of the nanopillar 16' is exposed by the removal of the excess material in accordance with processes discussed in relation to the structure illustrated in Figure 1(h) above.

The nanopillar 16' is then selectively etched, leaving an overlayer nanopore 52 as shown in Figure 3(f). The second overlayer 50, with overlayer nanopore 52, then acts as an etch mask for etching a nanopore 28' through the underlying stack 24' as illustrated in Figure 3(g). The second overlayer 50 is then etched to the top surface 54 of the stack as in Figure 3(h), producing a structure identical to that of Figure 1(i). From this point, one may proceed with the sequence of steps illustrated in Figures 1(j) through 1(m) to produce the transistor 36 of Figure 1(m). Alternatively, one may proceed from this point with the series of steps illustrated with reference to Figures

2(a) through 2(c) to produce the transistor 44 in accordance with an alternative embodiment of the invention.

5 Thus it is seen that the present invention provides a field effect transistor and a method for its manufacture that is both economical and advantageous in the resultant device. By forming a FET in accordance with the teachings of the invention, one may produce a device having an extremely narrow, yet well-defined
10 active channel. As such, problems such as high and variable series resistance and regions of abnormally high electric field are avoided.

15 By utilizing a nanoparticle etch mask, the costs associated with the high resolution photolithography are avoided. By forming the gate electrode (or gate electrode contact) of a conductive layer of material, within a stack that includes insulator layers, adjacent the vertically-oriented channel of the FET, the spacing of the gate from the
20 source or drain electrode formed at the upper surface of the underlying substrate is well defined.

25 While this invention has been defined with reference to its presently-preferred embodiment, it is not limited thereto. Rather, the invention is limited only insofar as it is defined by the following set of patent claims and includes within its scope all equivalents thereof.